WHAT IS CLAIMED IS:

1. A method of switching the mode of a PLL circuit, wherein the PLL circuit includes a phase comparator for comparing the phase of a reference frequency-divided signal and the phase of a comparison frequency-divided signal with each other and generating a comparison output signal, a charge pump for generating a current depending on the comparison output signal from the phase comparator, and a voltage-controlled oscillator for generating an output signal having a predetermined frequency in accordance with the current generated by the charge pump, and wherein the PLL circuit has a first mode for locking an output signal thereof up to a desired frequency at a high speed and a second mode in normal use, the method comprising the steps of:

detecting whether a current output terminal of the charge pump is in a high impedance state; and

switching the mode of the PLL circuit from the first mode to the second mode or from the second mode to the first mode when the high impedance state is detected.

2. The method of switching the mode of a PLL circuit according to claim 1, wherein the PLL circuit further includes a lock detecting circuit for detecting a locked state of the PLL circuit in accordance with the comparison output signal from the phase comparator and generating a lock detecting signal when the locked state is detected, a reference counter connected to the phase comparator, for generating the reference frequency-divided signal, a clock signal, and an internal state signal, and a main counter connected to the phase comparator, for generating the comparison frequency-divided signal, a clock signal, and an

internal state signal, the method further comprising the steps of:

controlling the lock detecting signal using the comparison output signal from the phase comparator and the clock signal and the internal state signal of either one of the reference counter and the main counter; and

generating a mode switching signal in accordance with the controlled lock detecting signal;

wherein the step of switching the mode of the PLL circuit includes switching the mode of the PLL circuit from the first mode to the second mode or from the second mode to the first mode in response to the mode switching signal.

3. The method of switching the mode of a PLL circuit according to claim 1, wherein the PLL circuit further includes a lock detecting circuit for detecting a locked state of the PLL circuit in accordance with the comparison output signal from the phase comparator and generating a lock detecting signal when the locked state is detected, a reference counter connected to the phase comparator, for generating the reference frequency-divided signal, a main counter connected to the phase comparator, for generating the comparison frequency-divided signal, and a shift register for generating a frequency-dividing ratio setting signal for changing a frequency-dividing ratio which is set by at least one of the reference counter and the main counter, the method further comprising the steps of:

controlling the lock detecting signal using the comparison output signal from the phase comparator and the frequency-dividing ratio setting signal; and

generating a mode switching signal in accordance with the controlled lock detecting signal;

wherein the step of switching the mode of the PLL circuit includes switching the mode of the PLL circuit from the first mode to the second mode or from the second mode to the first mode in response to the mode switching signal.

4. A circuit for controlling the mode of a PLL circuit, wherein the PLL circuit includes a phase comparator for comparing the phase of a reference frequency-divided signal and the phase of a comparison frequency-divided signal with each other and generating a comparison output signal, a charge pump connected to the phase comparator, for generating a current depending on the comparison output signal from the phase comparator, and a voltage-controlled oscillator connected to the charge pump, for generating an output signal having a predetermined frequency in accordance with the current generated by the charge pump, and wherein the PLL circuit has a first mode for locking an output signal thereof up to a desired frequency at a high speed and a second mode in normal use, the circuit comprising:

a state detecting circuit for detecting whether a current output terminal of the charge pump is in a high impedance state, and generating a mode switching signal to switch the mode of the PLL circuit from the first mode to the second mode or from the second mode to the first mode when the high impedance state is detected.

5. The circuit for controlling the mode of a PLL circuit according to claim 4, further comprising:

a lock detecting circuit connected to the state detecting circuit, for detecting a locked state of the PLL circuit in accordance with the comparison output signal

from the phase comparator and generating a lock detecting signal when the locked state is detected;

wherein the state detecting circuit generates the mode switching signal in accordance with the lock detecting signal.

6. The circuit for controlling the mode of a PLL circuit according to claim 5, wherein the PLL circuit includes a reference counter connected to the phase comparator, for generating the reference frequency-divided signal, a clock signal, and an internal state signal, and a main counter connected to the phase comparator, for generating the comparison frequency-divided signal, a clock signal, and an internal state signal; and wherein the state detecting circuit controls the lock detecting signal using the comparison output signal from the phase comparator and the clock signal and the internal state signal of either one of the reference counter and the main counter, and generates the mode switching signal in accordance with the controlled lock detecting signal.

7. The circuit for controlling the mode of a PLL circuit according to claim 6, wherein the phase comparator compares the phase of the reference frequency-divided signal and the phase of the comparison frequency-divided signal with each other and generates a first pulse signal and a second pulse signal, and wherein the state detecting circuit includes:

a first flip-flop for generating a first flip-flop output signal, the first flip-flop having a first clock input terminal for receiving the clock signal from the reference counter, a first data input terminal for receiving the internal state signal from the reference

counter, and a first reset input terminal for receiving the first pulse signal from the phase comparator;

a second flip-flop for generating a second flip-flop output signal, the second flip-flop having a second clock input terminal for receiving the clock signal from the main counter, a second data input terminal for receiving the internal state signal from the main counter, and a second reset input terminal for receiving the second pulse signal from the phase comparator;

an AND circuit connected to the first and second flip-flops, for receiving the first and second flip-flop output signals and generating an AND output signal; and

a latch circuit connected to the AND circuit and the lock detecting circuit, for latching the lock detecting signal in accordance with the AND output signal and generating the mode switching signal.

8. The circuit for controlling the mode of a PLL circuit according to claim 7, wherein each of the first and second flip-flops includes a D flip-flop.

9. The circuit for controlling the mode of a PLL circuit according to claim 6, wherein the reference counter generates the internal state signal thereof a predetermined number of clock pulses prior to the reference frequency-divided signal, and wherein the main counter generates the internal state signal thereof a predetermined number of clock pulses prior to the comparison frequency-divided signal.

10. The circuit for controlling the mode of a PLL circuit according to claim 6, wherein the state detecting circuit includes:

an AND circuit connected to the phase comparator, for receiving the first pulse signal and the second pulse signal and generating an AND output signal;

a flip-flop connected to the AND circuit, for generating a flip-flop output signal, the flip-flop having a clock input terminal for receiving the clock signal from the main counter, a data input terminal for receiving the internal state signal from the main counter, and a reset input terminal for receiving the AND output signal; and

a latch circuit connected to the flip-flop and the lock detecting circuit, for latching the lock detecting signal in accordance with the flip-flop output signal and generating the mode switching signal.

11. The circuit for controlling the mode of a PLL circuit according to claim 10, wherein the flip-flop includes a D flip-flop.

12. The circuit for controlling the mode of a PLL circuit according to claim 6, wherein the state detecting circuit includes:

an AND circuit connected to the phase comparator, for receiving the first pulse signal and the second pulse signal and generating an AND output signal;

a flip-flop connected to the AND circuit, for generating a flip-flop output signal, the flip-flop having a clock input terminal for receiving the clock signal from the reference counter, a data input terminal for receiving the internal state signal from the reference counter, and a reset input terminal for receiving the AND output signal; and

a latch circuit connected to the flip-flop and the lock detecting circuit, for latching the lock detecting

signal in accordance with the flip-flop output signal and generating the mode switching signal.

13. The circuit for controlling the mode of a PLL circuit according to claim 12, wherein the flip-flop includes a D flip-flop.

14. The circuit for controlling the mode of a PLL circuit according to claim 5, wherein the PLL circuit includes a reference counter for generating the reference frequency-divided signal, a main counter for generating the comparison frequency-divided signal, and a shift register connected to the reference counter and the main counter, for generating a frequency-dividing ratio setting signal for changing a frequency-dividing ratio which is set by at least one of the reference counter and the main counter, and wherein the state detecting circuit controls the lock detecting signal using the comparison output signal from the phase comparator and the frequency-dividing ratio setting signal, and generates the mode switching signal in accordance with the controlled lock detecting signal.

15. The circuit for controlling the mode of a PLL circuit according to claim 14, wherein the state detecting circuit includes:

an OR circuit connected to the phase comparator, for receiving the first pulse signal and the second pulse signal, and generating an OR output signal; and

a flip-flop connected to the OR circuit and the lock detecting circuit, for generating the mode switching signal, the flip-flop having a clock input terminal for receiving the OR output signal and a data input terminal for receiving the lock detecting signal, and a reset input

terminal for receiving the frequency-dividing ratio setting signal.

16. The circuit for controlling the mode of a PLL circuit according to claim 15, wherein the flip-flop includes a D flip-flop.

17. The circuit for controlling the mode of a PLL circuit according to claim 4, wherein the state detecting circuit further includes:

a delay circuit for delaying the mode switching signal by a predetermined time.

18. The circuit for controlling the mode of a PLL circuit according to claim 4, wherein the PLL circuit further includes a low-pass filter connected to the charge pump, for smoothing an output signal from the charge pump to remove high-frequency components therefrom, and supplying the output signal from the charge pump, from which the high-frequency components have been removed, to the voltage-controlled oscillator, and wherein the state detecting circuit supplies the mode switching signal to either one of the phase comparator, the charge pump, and the low-pass filter.

19. A semiconductor device comprising:

a PLL circuit; and

a mode control circuit connected to the PLL circuit, for controlling switching of the mode of the PLL circuit;

wherein the PLL circuit includes:

a phase comparator for comparing the phase of a reference frequency-divided signal and the phase of a

comparison frequency-divided signal with each other and generating a comparison output signal,

a charge pump connected to the phase comparator, for generating a current depending on the result of the comparison by the phase comparator, and

a voltage-controlled oscillator connected to the charge pump, for generating an output signal having a predetermined frequency in accordance with the current generated by the charge pump, wherein the PLL circuit has a first mode for locking an output signal thereof up to a desired frequency at a high speed and a second mode in normal use; and

wherein the mode control circuit detects whether a current output terminal of the charge pump is in a high impedance state, and generates a mode switching signal to switch the mode of the PLL circuit from the first mode to the second mode or from the second mode to the first mode when the high impedance state is detected.